2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91FY27U, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91FY27U.

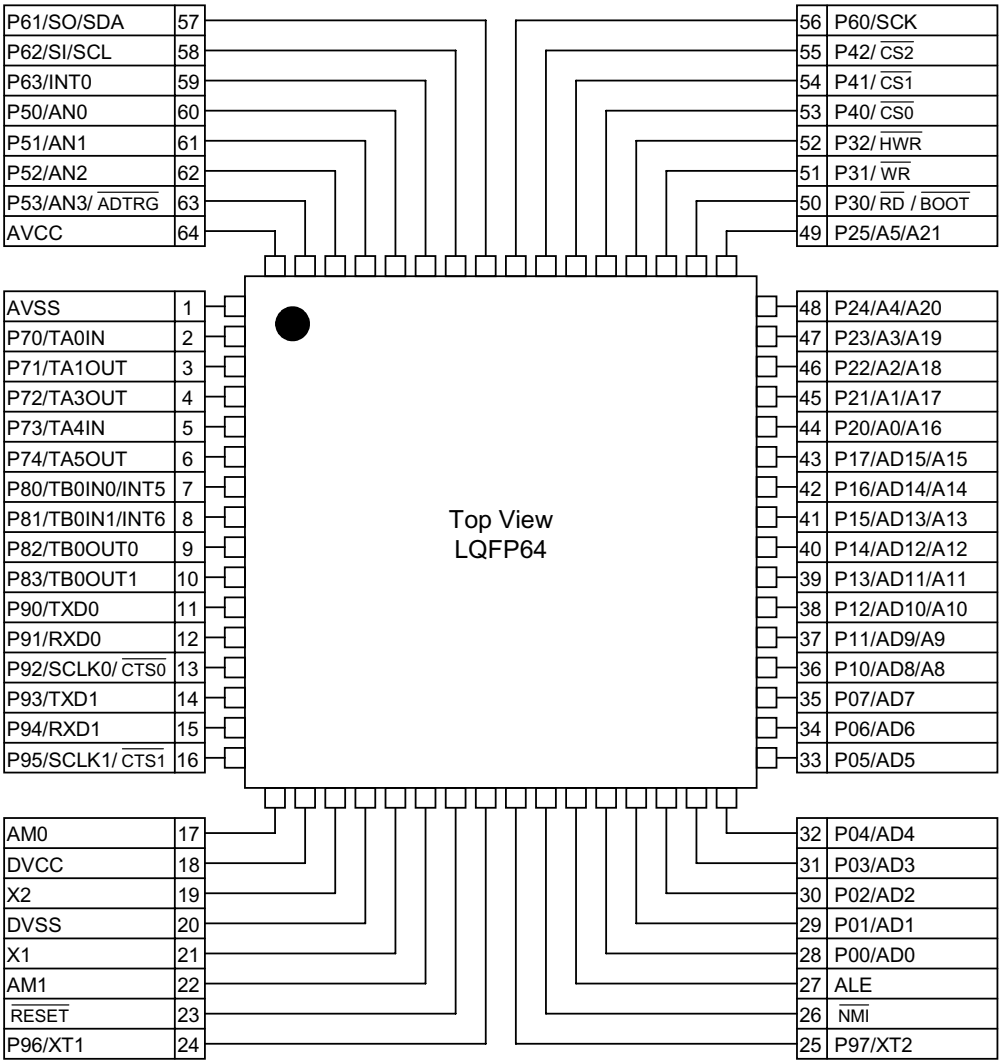

Figure 2.1.1 Pin Assignment Diagram (64-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below. Table 2.2.1 and Table 2.2.2 show Pin names and functions.

Table 2.2.1 Pin Names and Functions (1/2)

Pin Names	Number of Pins	I/O	Functions
P00 to P07	8	I/O	Port 0: I/O port that allows I/O to be selected at the bit level
AD0 to AD7		I/O	Address data (lower): 0 to 7 of address/data bus
P10 to P17	8	I/O	Port1: I/O port that allows I/O to be selected at the bit level
AD8 to AD15		I/O	Address data (upper): 8 to 15 of address/data bus
A8 to A15		Output	Address: 8 to 15 of address bus
P20 to P25	6	I/O	Port 2: I/O port that allows I/O to be selected at the bit level
A0 to A5		Output	Address: 0 to 5 of address bus
A16 to A21		Output	Address: 16 to 21 of address bus
P30	1	Output	Port 30: Output Port
$\overline{RD}$		Output	Read: Strobe signal for reading external memory When read internal area also, output $\overline{RD}$ by setting to P3<P30> = 0 and P3FC<P30F> = 1.
$\overline{BOOT}$		Input	This pin sets single boot mode (only during reset). For the details, please refer to section 3.1, “Outline of operation mode”.
P31	1	Output	Port 31: Output port
$\overline{WR}$		Output	Write: Strobe signal for writing data to pins AD0 to AD7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High Write: Strobe signal for writing data to pins AD8 to AD15
P40	1	I/O	Port 40: I/O port (with pull-up resistor)
$\overline{CS0}$		Output	Chip select 0: Outputs “0” when address is within specified address area.
P41	1	I/O	Port41: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip select 1: Outputs “0” when address is within specified address area.
P42	1	I/O	Port 42: I/O port (with pull-up resistor)
$\overline{CS2}$		Output	Chip select 2: Outputs “0” when address is within specified address area.
P50 to P53	4	Input	Port 5: Input port
AN0 to AN3		Input	Analog input: Analog input pins of the AD converter
$\overline{ADTRG}$		Input	AD trigger: Pin used to request AD start (shared with P53).
P60	1	I/O	Port 60: I/O port
SCK		I/O	Serial bus interface clock I/O at SIO mode
P61	1	I/O	Port 61: I/O port
SO		Output	Serial bus interface send data at SIO mode
SDA		I/O	Serial bus interface send/receive data at I^2C mode Open-drain output mode by programmable
P62	1	I/O	Port 62: I/O port
SI		Input	Serial bus interface receive data at SIO mode
SCL		I/O	Serial bus interface clock I/O at I^2C mode Open-drain output mode by programmable
P63	1	I/O	Port 63: I/O port (Schmitt input)
INT0		Input	Interrupt request pin 0: Interrupt request pin with level/ rising/falling edge
P70	1	I/O	Port 70: I/O port
TA0IN		Input	8-bit timer 0 input: Input pin of 8-bit timer TMRA0
P71	1	I/O	Port 71: I/O port
TA1OUT		Output	8-bit timer 1 output: Output pin of 8-bit timer TMRA0 or TMRA1
P72	1	I/O	Port 72: I/O port
TA3OUT		Output	8-bit timer 3 output: Output pin of 8-bit timer TMRA2 or TMRA3

Table 2.2.2 Pin Names and Functions (2/2)

Pin Names	Number of Pins	I/O	Functions
P73 TA4IN	1	I/O Input	Port 73: I/O port 8-bit timer 4 Input: Input pin of 8-bit timer TMRA4
P74 TA5OUT	1	I/O Output	Port 74: I/O port 8-bit timer 5 output: Output pin of 8-bit timer TMRA4 or TMRA5
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port 16-bit timer 0 Input 0: Input of count/capture trigger in 16-bit timer TMRB0 Interrupt request pin 5: Interrupt request pin with selectable rising/falling edge
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port 16-bit timer 0 Input 1: Input of count/capture trigger in 16-bit timer TMRB0 Interrupt request pin 6: Interrupt request pin of rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port 16-bit timer 0 output 0: Outpit pin of 16-bit timer TMRB0
P83 TB0OUT1	1	I/O Output	Port 83: I/O port 16-bit timer 0 output 1: Output pin of 16-bit timer TMRB0
P90 TXD0	1	I/O Output	Port 90: I/O port Serial 0 send data: Open-drain output pin by programmable
P91 RXD0	1	I/O Input	Port 91: I/O port Serial 0 receive data
P92 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port 92: I/O port Serial 0 clock I/O Serial 0 data send enable (Clear to send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial 1 send data: Open-drain output pin by programmable
P94 RXD1	1	I/O Input	Port 94: I/O port Serial 1 receive data
P95 SCLK1 $\overline{\text{CTS1}}$	1	I/O I/O Input	Port 95: I/O port Serial 1 clock I/O Serial 1 data send enable (Clear to send)
P96 XT1	1	I/O Input	Port 96: I/O port. Open-drain output pin. Low frequency oscillator connection pin
P97 XT2	1	I/O Output	Port 97: I/O port. Open-drain output pin. Low frequency oscillator connection pin
ALE	1	Output	Address latch enable (It can be set as prohibition of an output for noize reduction.)
$\overline{\text{NMI}}$	1	Input	Non-Maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable (Schmitt input).
AM0 and AM1	2	Input	Operation mode: Fixed to AM1 = “1” and AM0 = “1”.
$\overline{\text{RESET}}$	1	Input	Reset: Initialize LSI. (Schmitt input, with pull-up resistor)
AVCC	1		Pin used to both power supply pin for AD converter and standard power supply for AD converter (H).
AVSS	1		Pin used to both GND pin for AD converter (0 V) and standard power supply pin for AD converter (L).
X1/X2	2	I/O	High frequency oscillator connection pin.
DVCC DVSS	1 1		Power supply pins (All DVCC pins should be connected with the power Supply pin). GND pins (All pins shuold be connected with GND(0V).)